Claims

What is claimed is:

1. A radio frequency (RF) converter system for generating RF signals, comprising:

a signal conversion circuit for at least one of digital signal processing (DSP) and converting between digital signals and analog signals;

a shifting circuit in communication with the signal conversion circuit for at least one of frequency shifting and phase shifting at least one of the digital signals and analog signals, as a function of at least one of an oscillating signal and a baseband signal to generate modulated signals; and

a termination circuit in communication with the shifting circuit for transmitting a portion of the modulated signals;

wherein a frequency associated with the at least one of the oscillating signal and the baseband signal, a frequency associated with the termination circuit, a frequency corresponding to a clock associated with the signal conversion circuit, and a frequency associated with a master clock are integer multiples of each other.

2. An RF converter system as recited in claim 1, wherein an output of the termination circuit is isolated from an input thereof.

3. An RF converter system as recited in claim 1, wherein a frequency locking circuit ensures that the frequency associated with the oscillating signal, the frequency associated with the termination circuit , the frequency corresponding to the clock associated with the signal conversion circuit, and the frequency associated with the master clock are integer multiples of each other.

4. An RF converter system as recited in claim 1, wherein an input of the

termination circuit has a reference that is common with an input of the shifting circuit.

5. An RF converter system as recited in claim 1, wherein the shifting circuit is directly connected to the signal conversion circuit.

6. An RF converter system as recited in claim 1, wherein a polarity of a current from the signal conversion circuit is reversed to match a polarity of a current to the shifting circuit.

7. An RF converter system as recited in claim 1, wherein the oscillating signal associated with the shifting circuit and an input of the termination circuit have a reference that is common

8. An RF converter system as recited in claim 7, wherein the reference is adjustable

9. An RF converter system as recited in claim 1, wherein a DC biasing current flowing into the shifting circuit is adjustable, zero inclusive.

10. An RF converter system as recited in claim 1, wherein a DC biasing current flowing into the shifting circuit is set equal to a full scale current value of the signal conversion circuit.

11. An RF converter system as recited in claim 1, wherein the integer multiple is a less than one (1) such that the frequency associated with the oscillating signal, the frequency associated with the termination circuit, the frequency corresponding to the clock associated with the signal conversion circuit, and the frequency associated with the master clock are integer divisor of each other.

12. An RF converter system as recited in claim 1, wherein the integer multiple includes one (1).

13. An RF converter system as recited in claim 1, wherein the signal conversion circuit, the shifting circuit, and the termination circuit are stacked between supply rails.

14 An RF converter system as recited in claim 1, wherein a plurality of shifting circuits and termination circuits are included.

15. An RF converter system as recited in claim 14, wherein the signal conversion circuit, the shifting circuits, and the termination circuit are stacked between supply rails.

16. An RF converter system as recited in claim 1, wherein at least one of the circuits includes a folded circuit with passive current polarity reversing circuits facilitating current folding.

17. An RF converter system as in claim 16, wherein the passive current polarity reversing circuits possess a current gain of one (1) inclusive.

18. An RF converter system as recited in claim 1, wherein at least one of the circuits includes a folded circuit with active current polarity reversing circuits facilitating current folding.

19. An RF converter system as in claim 18, wherein the active current polarity reversing circuits possess a current gain of one (1) inclusive.

20. An RF converter system as recited in claim 1, wherein at least one of the circuits includes a low voltage standing wave ratio (VSWR) current input circuit.

21. An RF converter system as recited in claim 1, wherein at least one of the circuits includes a low headroom current input circuit.

22. An RF converter system as recited in claim 1, wherein at least one of the circuits includes a multiple input current mode circuit.

23. An RF converter system as recited in claim 1, wherein at least one of the circuits includes a voltage mode input circuit with conversion gain.

24. An RF converter system as recited in claim 1, wherein at least one of the circuits includes a multiple-mode circuit which operates in a voltage mode and a current mode simultaneously.

25. An RF converter system as recited in claim 1, and further comprising dual, phase adjustable, direct digital synthesis (DDS) devices, with phase adjustments offset 90 degrees; dual RF digital-to-analog devices (DACs), with at least 2 bits of resolution, that share a common frequency locking device; a common frequency locking circuit that has dual outputs to drive baseband DACs and DDS engines; and a common frequency locking circuit that has dual outputs to drive a local oscillator port of the RFDACs.

26. An RF converter system as recited in claim 1, and further comprising: 0 and 90 degree phase offset baseband digital engines driving respective RF digital-to-analog devices (DACs), that share a common zero (0) degree phase offset local oscillator driven frequency locking device; a common frequency locking circuit that has dual outputs to the RFDACs and digital engines; dual frequency locking circuits driven by 0 and 90 degree phase offset local oscillators, the 0 degree phase offset local oscillator driving the local oscillator port of the 0 degree phase offset baseband digital engine and RFDAC, and the 90 dgree phase offset local oscillator driving the local oscillator port

of the 90 degree phase offset baseband digital engine and RFDAC; the RFDAC outputs summed to produce a phase cancelled, single sideband output.

27. An RF converter system as recited in claim 1, wherein the signal conversion circuit includes a digital-to-analog (DAC), and the shifting circuit shifts the analog signals.

28. An RF converter system as recited in claim 1, wherein the signal conversion circuit includes an analog-to-digital (ADC), and the shifting circuit shifts the digital signals.

29 An RF converter system as recited in claim 1, wherein the signal conversion circuit includes a digital signal processor (DSP), and the shifting circuit shifts the digital signals.

30. A RF converter system as recited in claim 1, wherein the signal conversion circuit and the shifting circuit are combined into a single unit separate from the termination circuit.

31. A RF converter system as recited in claim 1, wherein a frequency locking circuit ensures that the frequency associated with the oscillating signal, the frequency associated with the termination circuit, the frequency corresponding to the clock associated with the signal conversion circuit, and the frequency associated with the master clock are integer multiples of each other; and divide and/or multiply integer ratios of the frequency locking circuit and the termination circuit are changed so as to maintain integer frequency relationships.

32. A RF converter system as recited in claim 1, wherein the termination circuit is actively operated.

33. A RF converter system as recited in claim 1, wherein the termination circuit is passively operated.

34. An RF Converter system as recited in claim 1, wherein the termination circuit is a wire.

35. An RF converter system as recited in claim 1, wherein the oscillating signal associated with the shifting circuit and an input of the termination circuit have references that are offset with respect to each other.

36. A method for generating radio frequency (RF) signals, comprising:

at least one of digitally processing and converting between digital signals and analog signals;

at least one of frequency shifting and phase shifting at least one of the digital signals and analog signals, as a function of at least one of an oscillating signal and a baseband signal to generate modulated signals; and

transmitting a portion of the modulated signals;

wherein a frequency associated with the at least one of the oscillating signal and the baseband signal, a frequency associated with the output signal, a frequency corresponding to a clock signal associated with the converting, and a frequency associated with a master clock are integer multiples of each other.

37. A method as recited in claim 36, wherein a baseband spectrum of the converted signals is directly upconverted and split into sum and difference spectrums, centered around the oscillating signal and harmonics thereof.

38. A method as recited in claim 36, wherein a baseband fundamental and a first Nyquist zone of the converted signals are directly upconverted and split into sum and

difference frequencies and spectrums, thereby being virtually amplified, centered adjacent to the oscillating signal and harmonics thereof.

39. A method as recited in claim 36, wherein aliases of the converted signals are directly upconverted and split into sum and difference frequencies, thereby being virtually amplified, centered around the oscillating signal and harmonics thereof.

40. A method as recited in claim 36, wherein aliases and a spectrum of the converted signals in close proximity to the oscillating signal and harmonics thereof are directly downconverted and upconverted and split into sum and difference spectrums, thereby being virtually attenuated, centered around a direct current (DC) of the oscillating signal and the harmonics thereof.

41. A method as recited in claim 36, wherein the output signal is filtered by a termination circuit that is frequency locked and bounded to the oscillating signal and a system sampling clock by the relationship: N*LO+Z*(Fs/2), where the LO includes the oscillating signal, Fs includes a frequency of a system sampling clock, the N, and Z are non-zero, independent integers.

42. A method as recited in claim 36, wherein the output signal is filtered by a termination circuit that is frequency locked and bounded to the oscillating signal and a system sampling clock by the relationship: N*LO-Z*(Fs/2), where the LO includes the oscillating signal, Fs includes a frequency of a system sampling clock; and the N, and Z are non-zero, independent integers.

43. A method as recited in claim 36, wherein the output signal is filtered by a termination circuit that is frequency locked and bounded to the oscillating signal and a system sampling clock by the relationship: [N*LO+Z*(Fs/2)]+[Z*(Fs/2)+Z*Fs], where the LO includes the oscillating signal, Fs includes a frequency of a system sampling

clock; and the N, and Z are non-zero, independent integers.

44. A method as recited in claim 36, wherein the output signal is filtered by a termination circuit that is frequency locked and bounded to the oscillating signal and a system sampling clock by the relationship: N*LO-Z*(Fs/2)]-[Z*(Fs/2)-Z*Fs], where the LO includes the oscillating signal, Fs includes a frequency of a system sampling clock; and the N, and Z are non-zero, independent integers.

45. A method as recited in claim 36, and further comprising:

tuning a dual direct digital synthesis (DDS) engine to a 90 degrees offset;

tuning the DDS engine to a frequency that is 1/4 a baseband digital-to-analog (DAC) clock (Fs) rate;

tuning a RFDAC frequency locking device and a termination circuit to select a desired frequency output; and

re-tuning the DDS engine to compensate for delay or phase inaccuracies in analog portions of the RFDAC.

46. A method as recited in claim 36, wherein the output signal is directly transmitted without frequency selection.

47. A radio frequency (RF) converter system for receiving RF signals, comprising:

a signal conversion circuit for at least one of digital signal processing (DSP) and converting between digital signals and analog signals;

a shifting circuit in communication with the signal conversion circuit for at least one of frequency shifting and phase shifting at least one of the digital signals and analog signals, as a function of at least one of an oscillating signal and a baseband signal to generate direct current signals;

a port in communication with the output of the shifting circuit for communicating modulated signals, and

a termination circuit in communication with the shifting circuit and the port, for receiving a portion of the direct current and the modulated signals;

wherein a frequency associated with the at least one of the oscillating signal and the baseband signal, a frequency associated with the termination circuit, a frequency corresponding to a clock associated with the signal conversion circuit, and a frequency associated with a master clock are integer multiples of each other.

48. An RF converter system as recited in claim 47, wherein an output of the termination circuit is isolated from an input thereof.

49. An RF converter system as recited in claim 47, wherein a frequency locking circuit ensures that the frequency associated with the oscillating signal, the frequency associated with the termination circuit , the frequency corresponding to the clock associated with the signal conversion circuit, and the frequency associated with the master clock are integer multiples of each other.

50. An RF converter system as recited in claim 47, wherein an input of the termination circuit has a reference that is common with an input of the shifting circuit.

51. An RF converter system as recited in claim 47, wherein the shifting circuit is directly connected to the signal conversion circuit.

52 An RF converter system as recited in claim 47, wherein a polarity of a current from the signal conversion circuit is reversed to match a polarity of a current to the shifting circuit.

53. An RF converter system as recited in claim 47, wherein the oscillating signal associated with the shifting circuit and an input of the termination circuit have a reference that is common.

54. An RF converter system as recited in claim 53, wherein the reference is adjustable.

55. An RF converter system as recited in claim 47, wherein a DC biasing current flowing into the shifting circuit is adjustable, zero inclusive.

56. An RF converter system as recited in claim 47, wherein a DC biasing current flowing into the shifting circuit is set equal to a full scale current value of the signal conversion circuit.

57. An RF converter system as recited in claim 47, wherein the integer multiple is a less than one (1) such that the frequency associated with the oscillating signal, the frequency associated with the termination circuit, the frequency corresponding to the clock associated with the signal conversion circuit, and the frequency associated with the master clock are integer divisor of each other.

58. An RF converter system as recited in claim 47, wherein the integer multiple includes one (1).

59. An RF converter system as recited in claim 47, wherein the signal conversion circuit, the shifting circuit, and the termination circuit are stacked between supply rails.

60. An RF converter system as recited in claim 47, wherein at least one of the circuits includes a low voltage standing wave ratio (VSWR) current input circuit.

61. An RF converter system as recited in claim 47, wherein at least one of the circuits includes a low headroom current input circuit.

62. An RF converter system as recited in claim 47, wherein at least one of the circuits includes a multiple input current mode circuit.

63. An RF converter system as recited in claim 47, wherein at least one of the circuits includes a voltage mode input circuit with conversion gain.

64. An RF converter system as recited in claim 47, wherein at least one of the circuits includes a multiple-mode circuit which operates in a voltage mode and a current mode simultaneously.

65. An RF converter system as recited in claim 47, wherein the signal conversion circuit includes a digital-to-analog (DAC), and the shifting circuit shifts the analog signals.

66. A RF converter system as recited in claim 47, wherein the signal conversion circuit, the shifting circuit, and the termination circuit are combined into a single unit.

67. A RF converter system as recited in claim 47, wherein a frequency locking circuit ensures that the frequency associated with the oscillating signal, the frequency associated with the termination circuit, the frequency corresponding to the clock associated with the signal conversion circuit, and the frequency associated with the master clock are integer multiples of each other; and divide and/or multiply integer ratios of the frequency locking circuit and the termination circuit are changed so as to maintain integer frequency relationships.

68. A RF converter system as recited in claim 47, wherein the termination circuit is actively operated.

69. A RF converter system as recited in claim 47, wherein the termination circuit is

passively operated.

70. An RF converter system as recited in claim 47, wherein the oscillating signal associated with the shifting circuit and an input of the termination circuit have references that are offset with respect to each other.

71. A method for receiving radio frequency (RF) signals, comprising:

receiving a non-varying direct current signal from a signal conversion circuit adapted for signal conversion, where the direct current signal serves to nullify an oscillating signal applied to a shifting circuit and provide biasing for a termination circuit; and

combining the non-varying direct current signal with incoming modulated signals from a transmit/receive port for application to the termination circuit, where the termination circuit is adapted for generating baseband signals as a function of the oscillating signal;

wherein a frequency associated with the at least one of the oscillating signal and the baseband signals, a frequency associated with an output signal, a frequency corresponding to a clock signal associated with the signal conversion, and a frequency associated with a master clock signal are integer multiples of each other.